

Fig. 1

FIG. 2 is a schematic diagram of a system 200, which includes a plurality of input nodes 120, 160, and 170, a plurality of output nodes 110, 160, and 170, and a plurality of processing nodes 240. The input nodes 120, 160, and 170 are connected to the processing nodes 240, which are in turn connected to the output nodes 110, 160, and 170.

200

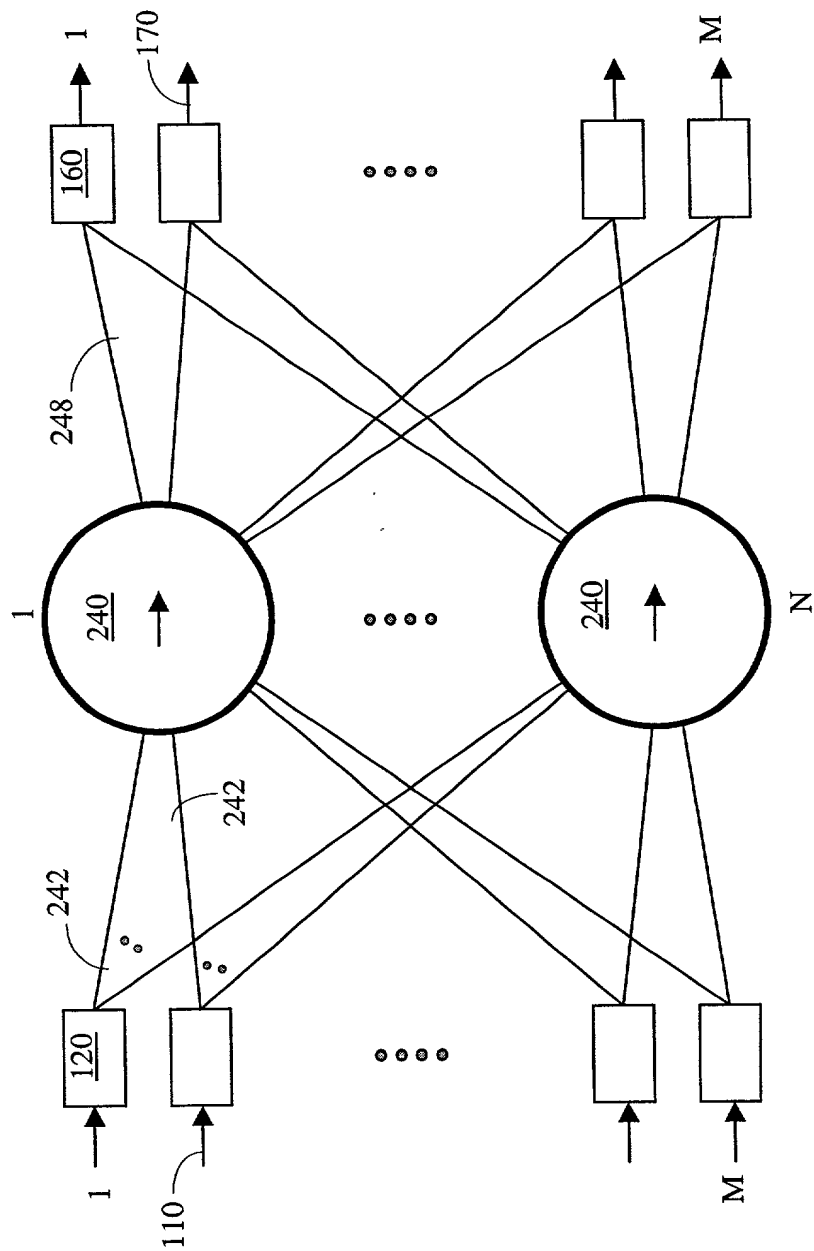


Fig. 2

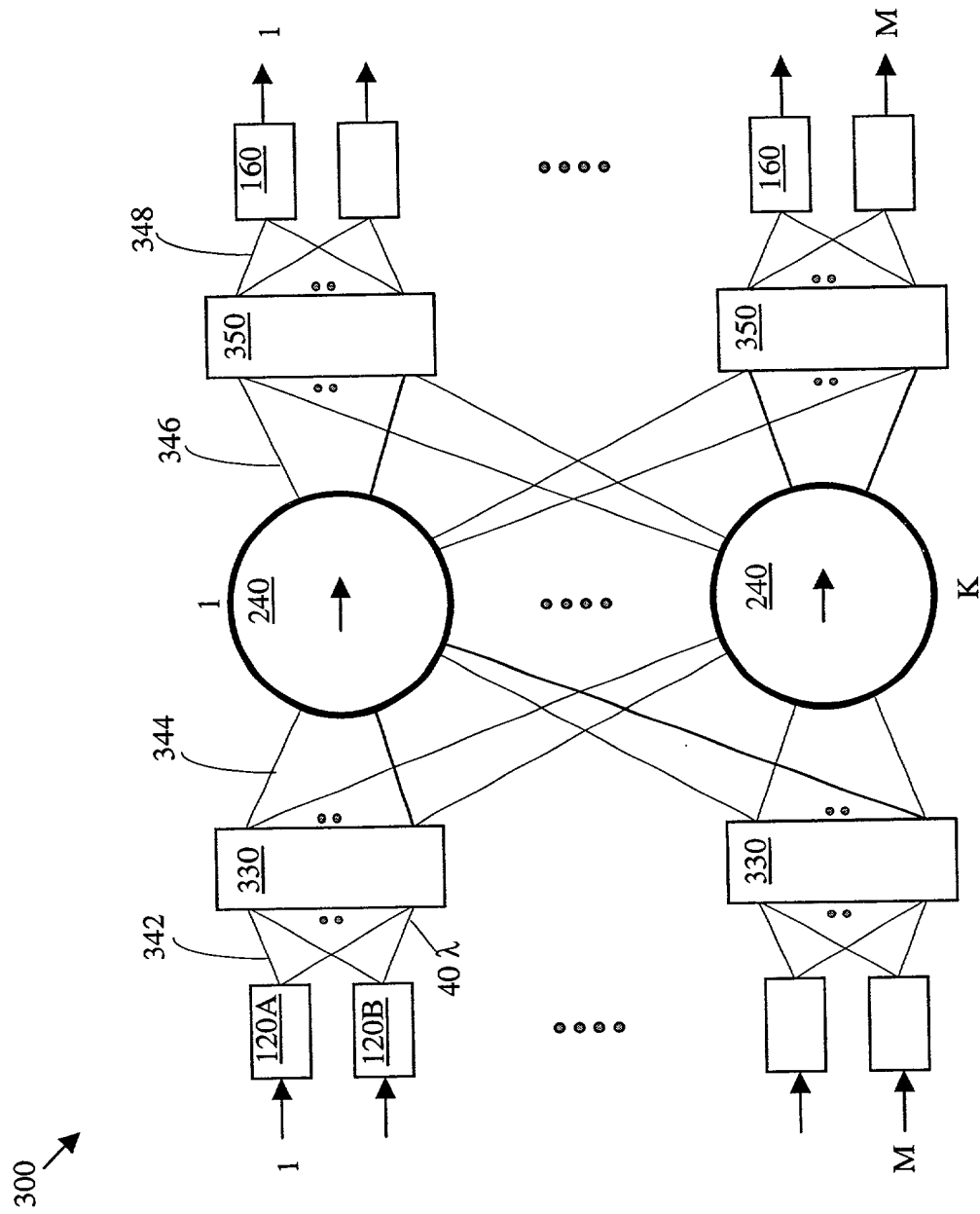


Fig. 3

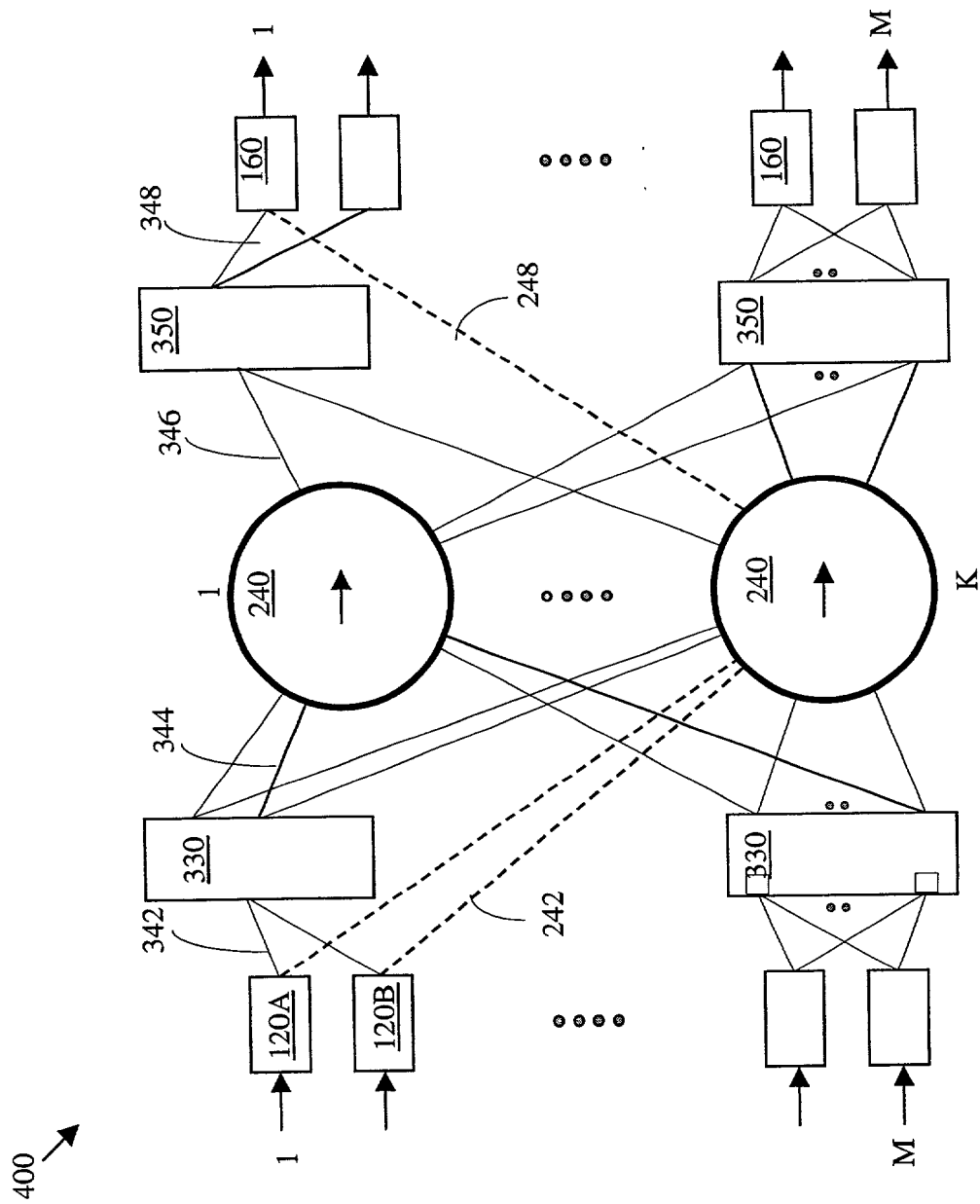


Fig. 4

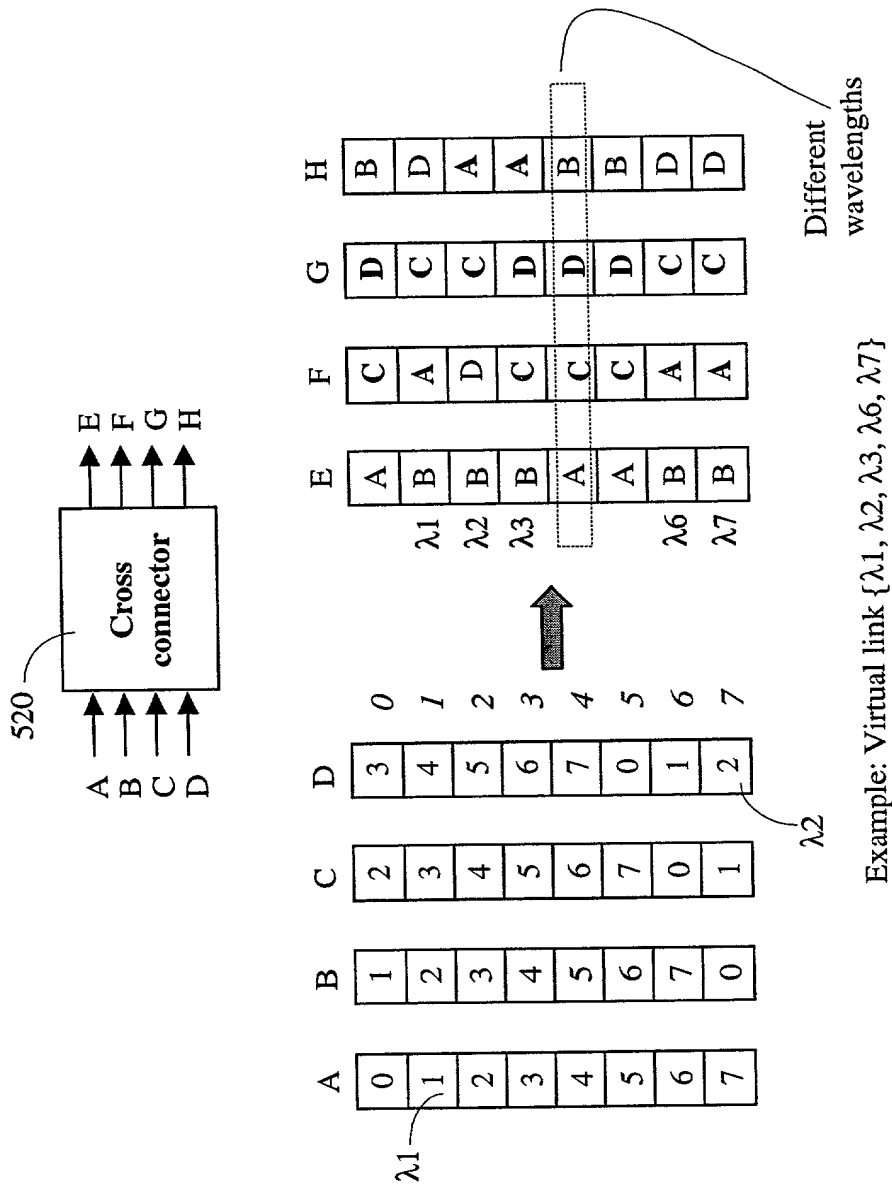


Fig. 5

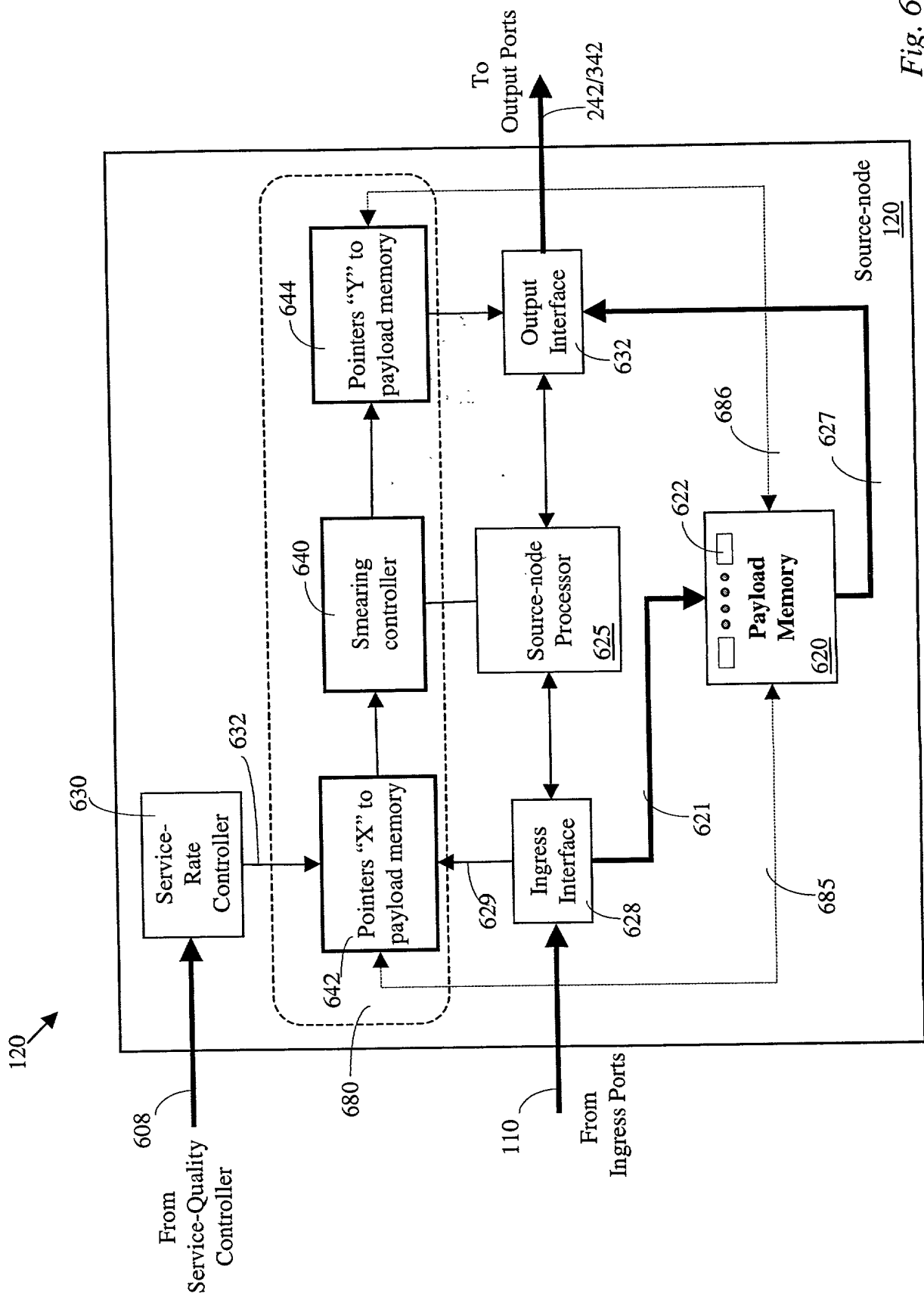


Fig. 6

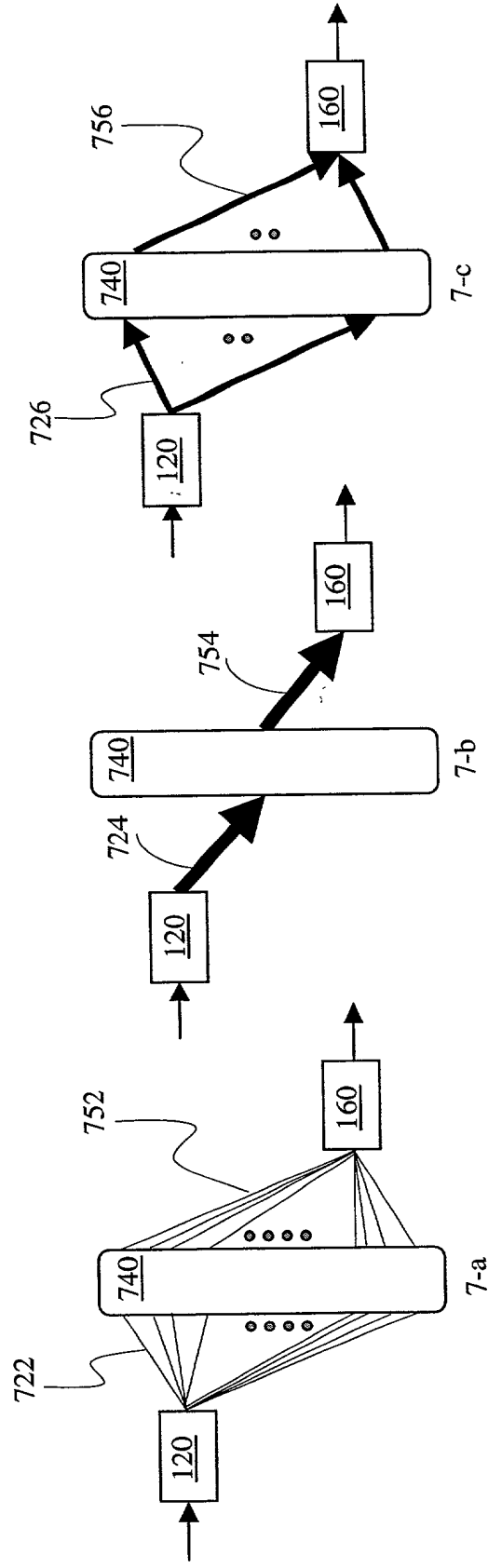


Fig. 7

FIG. 8 is a schematic diagram of a core space switch system. The system includes a core space switch 840, which is a $(W \times N) \times (W \times N)$ switch. The switch is connected to two links, Link-A and Link-B. Link-A is connected to a source 110 and a destination 120. Link-B is connected to a source 160 and a destination 170. The switch 840 has a central core 830 and two sets of input/output ports, 822 and 823, which are connected to the links. The switch 840 is also connected to a set of output ports 850. The switch 840 is a $(W \times N) \times (W \times N)$ switch, where W is the number of wavelengths and N is the number of nodes.

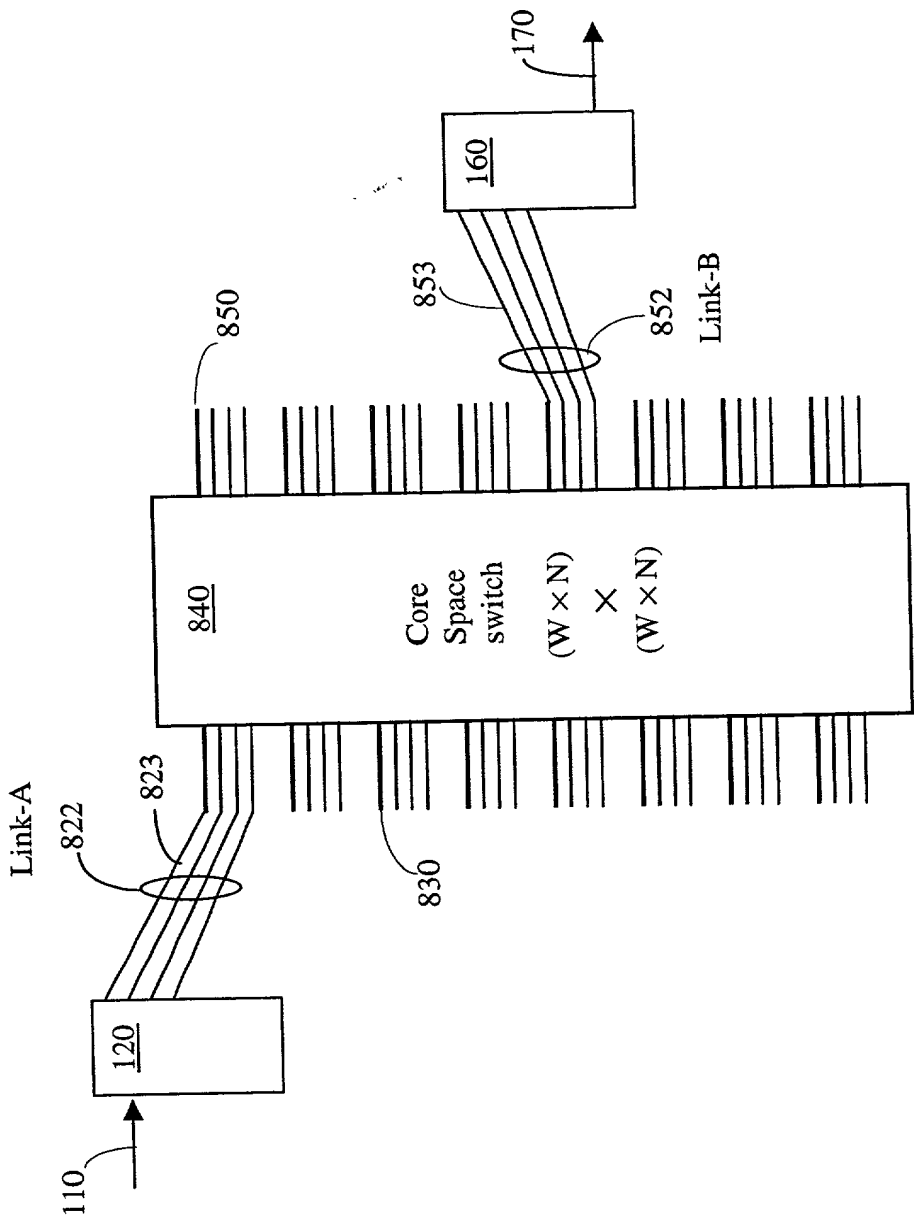


Fig. 8

1. *Staphylococcus aureus* (1000)
 2. *Staphylococcus aureus* (1000)
 3. *Staphylococcus aureus* (1000)
 4. *Staphylococcus aureus* (1000)
 5. *Staphylococcus aureus* (1000)
 6. *Staphylococcus aureus* (1000)
 7. *Staphylococcus aureus* (1000)
 8. *Staphylococcus aureus* (1000)
 9. *Staphylococcus aureus* (1000)
 10. *Staphylococcus aureus* (1000)

Fig. 9

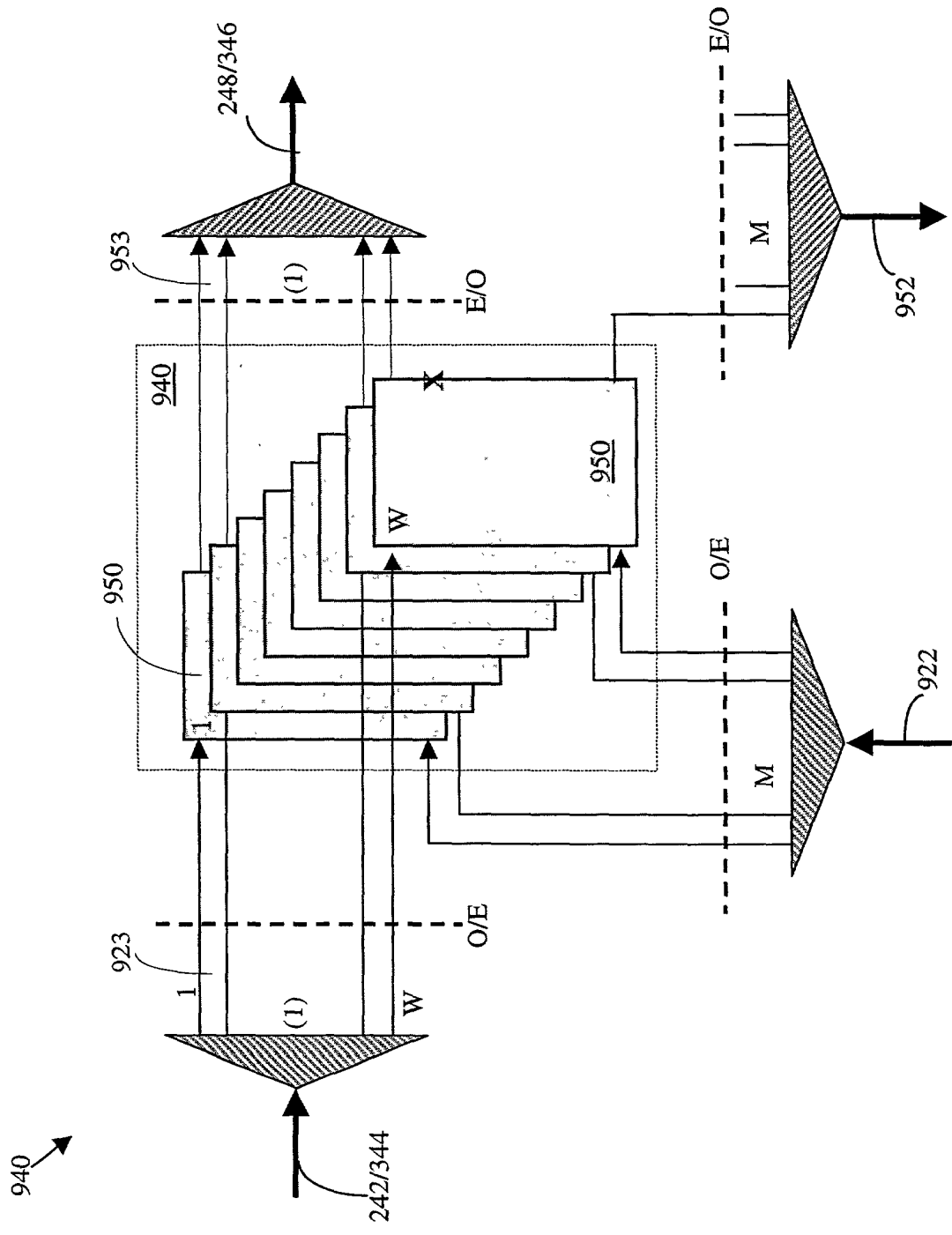


Fig. 10

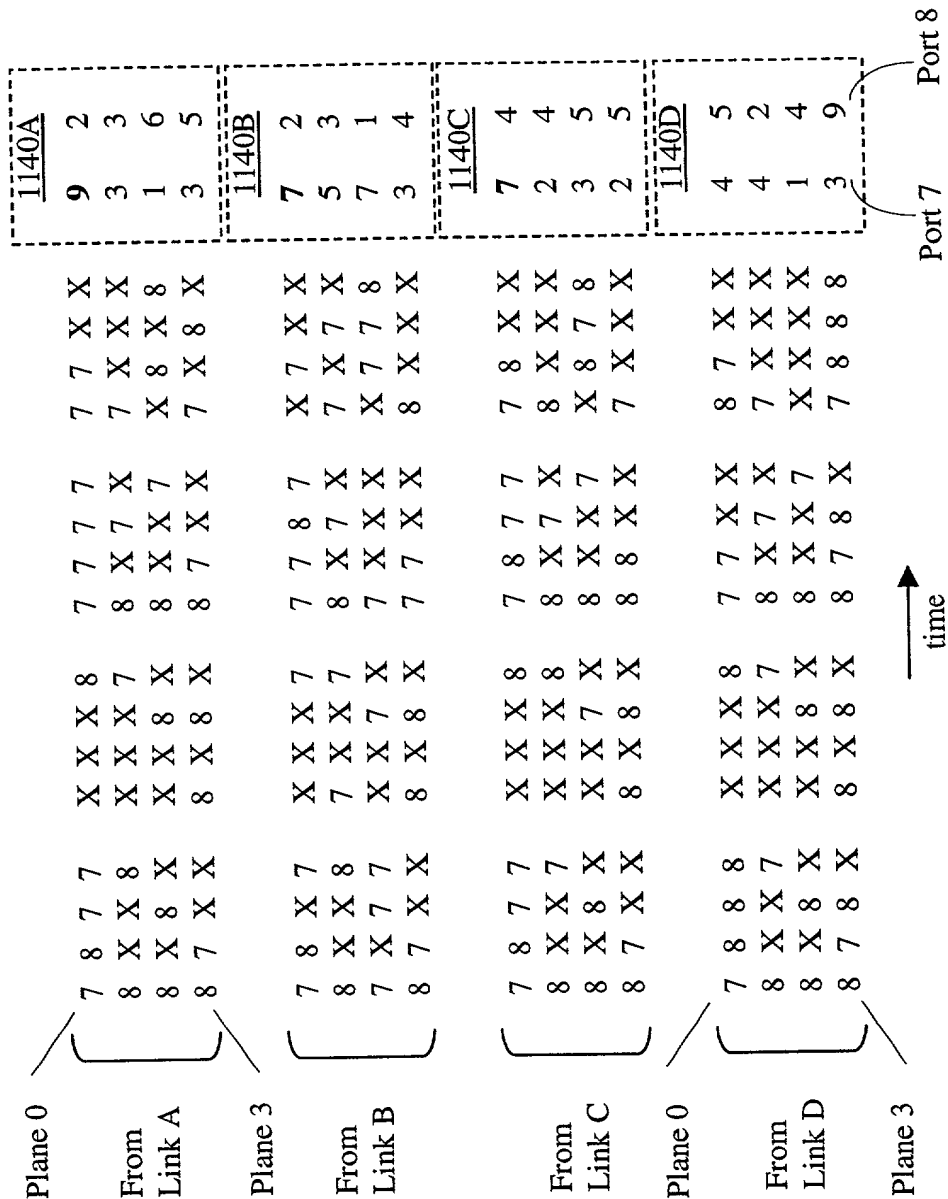


Fig. 11a

1160 ↗

	Port 7	Port 8
Link-A	16	16
Link-B	22	10
Link-C	14	18
Link-D	12	20
	64	64

Fig. 11b

1180 ↘

	Port 7	Port 8
Plane-0	27	13
Plane-1	14	12
Plane-2	12	16
Plane-3	11	23
	64	64

Fig. 11c

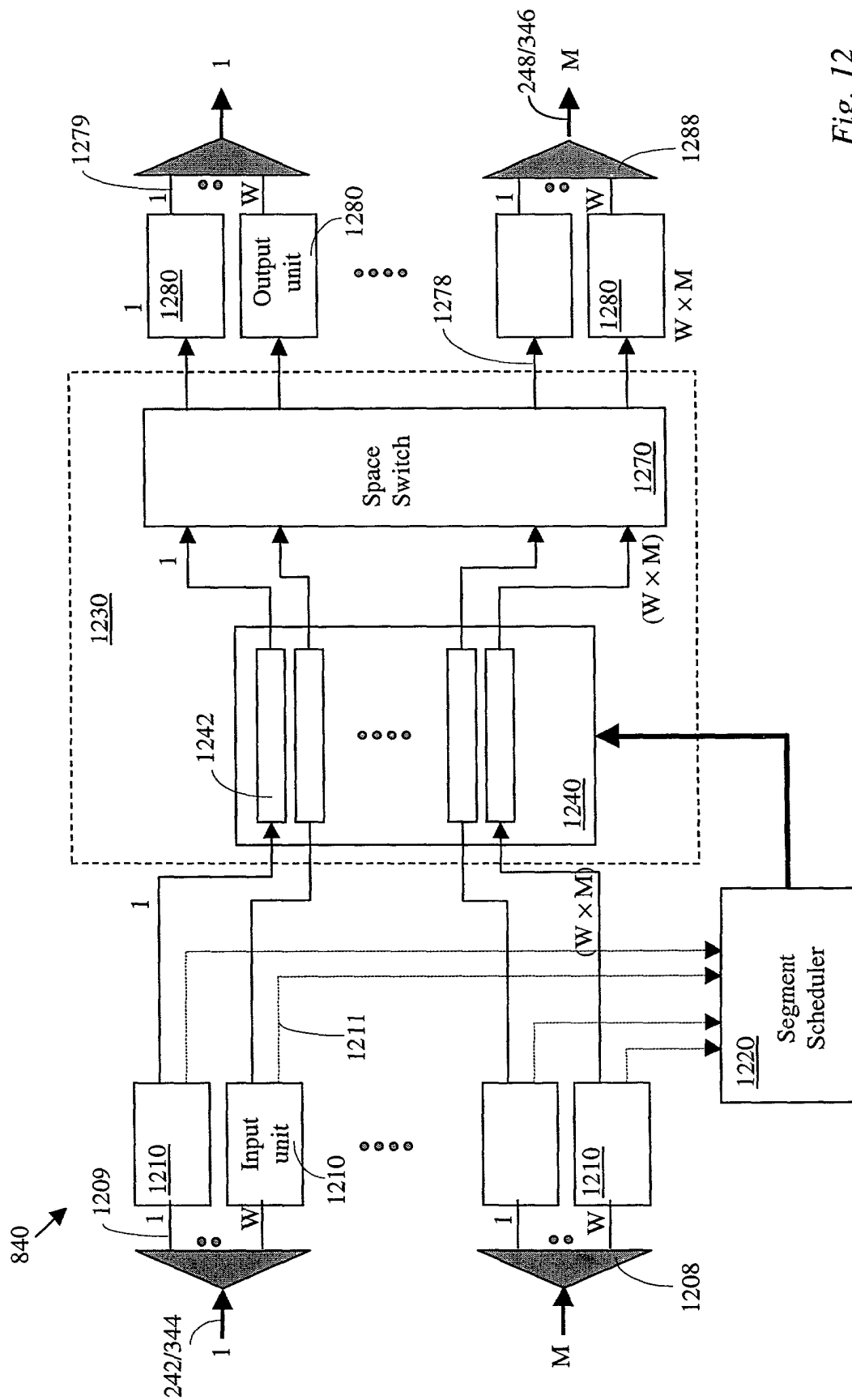


Fig. 12

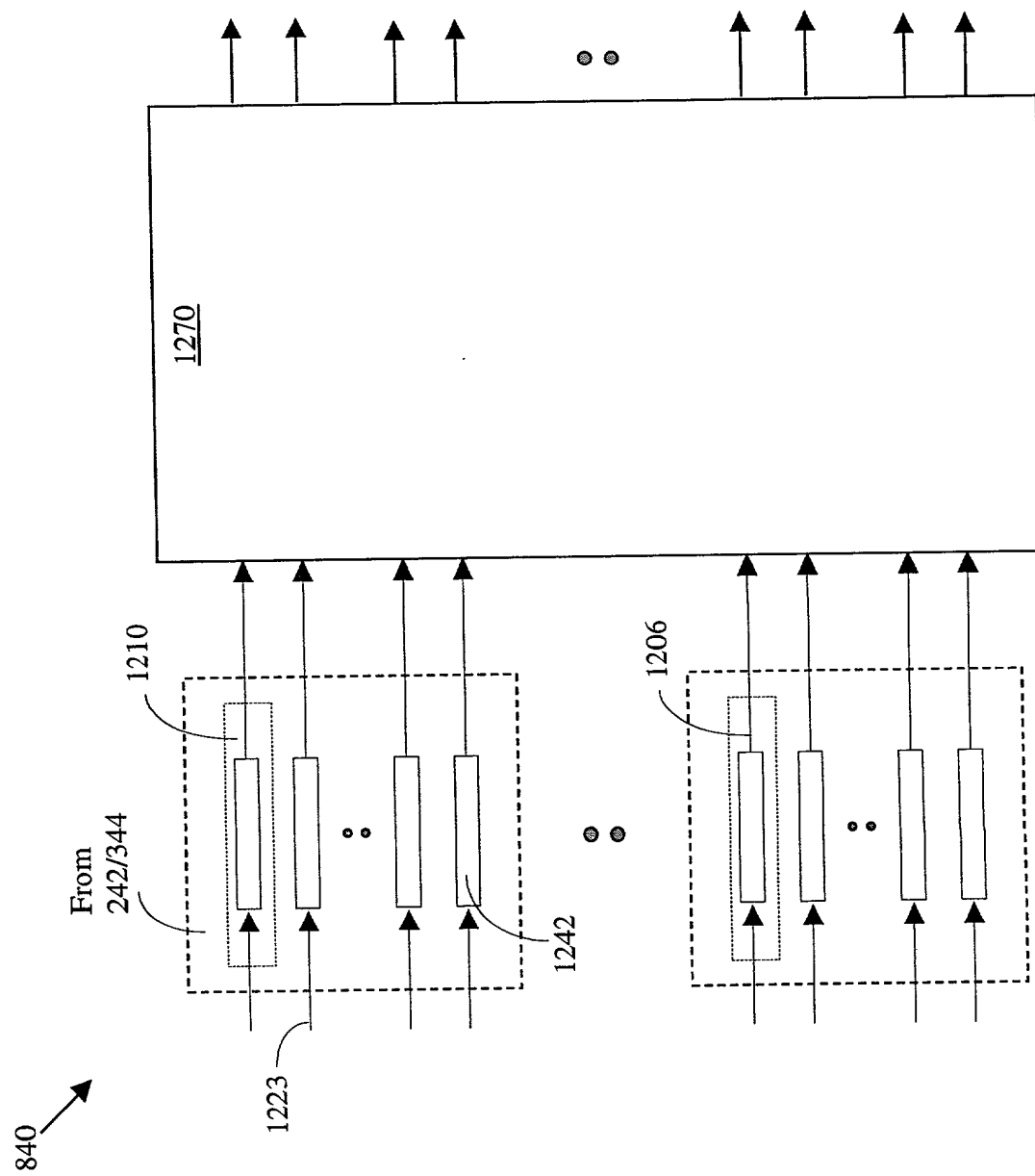


Fig. 13

940

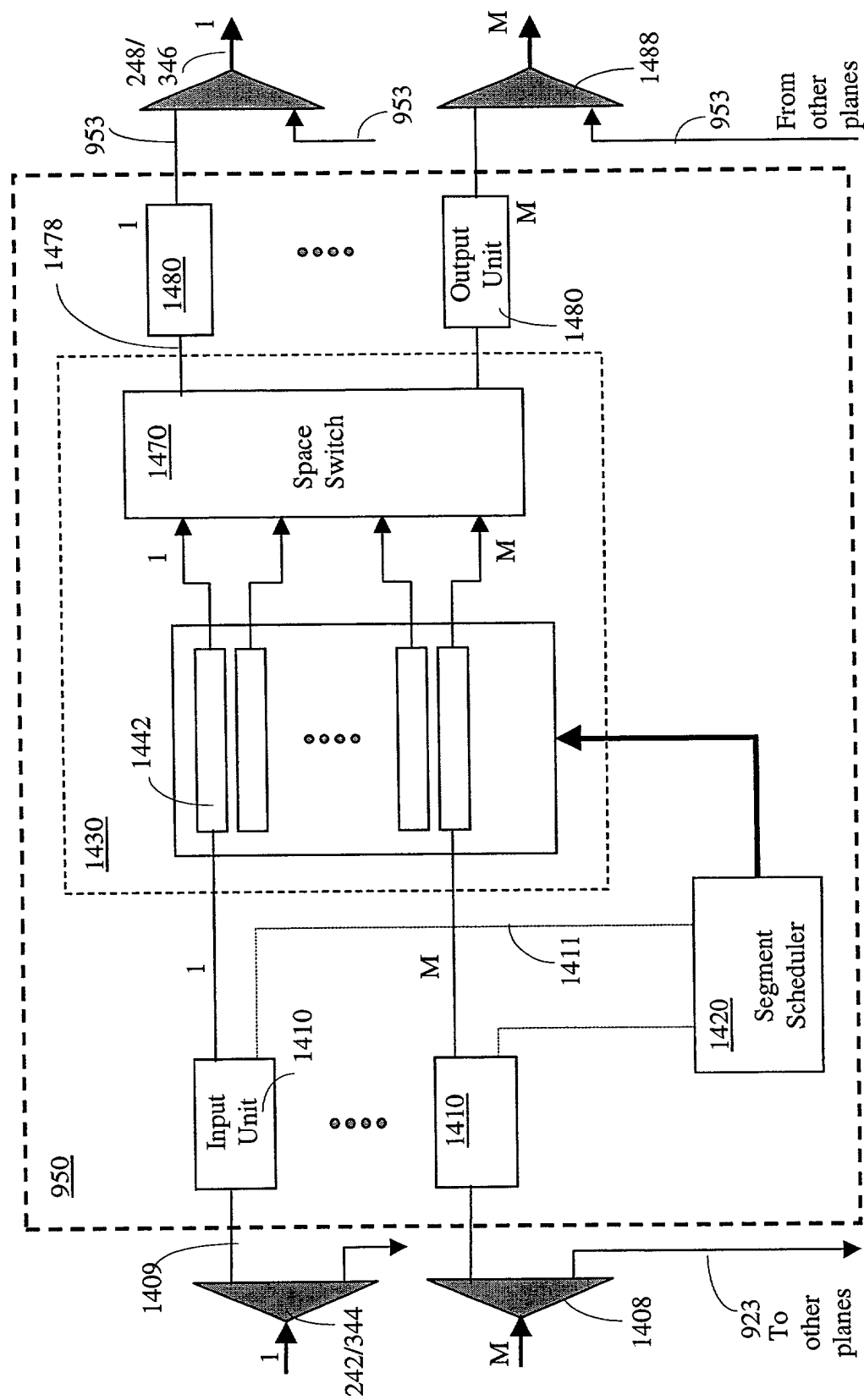


Fig. 14

FIG. 15 is a block diagram of a system 1430, according to one embodiment of the present invention. The system 1430 includes a plurality of processing units 1442, each of which is connected to a corresponding output unit 1470. The output units 1470 are connected to a common output bus 1478. The system 1430 is configured to process data received from a data source (not shown) and output the processed data to the output bus 1478.

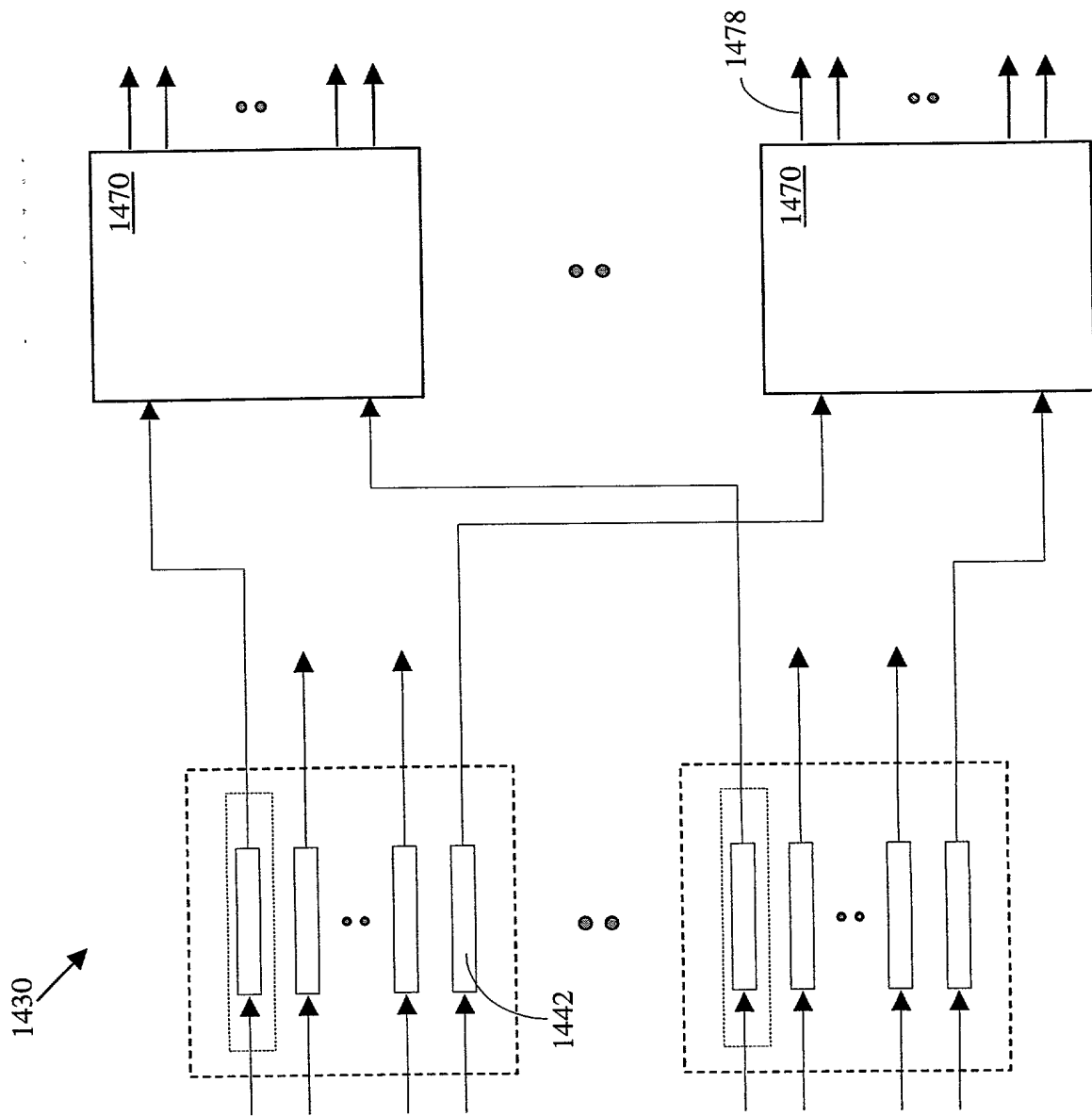


Fig. 15

1600

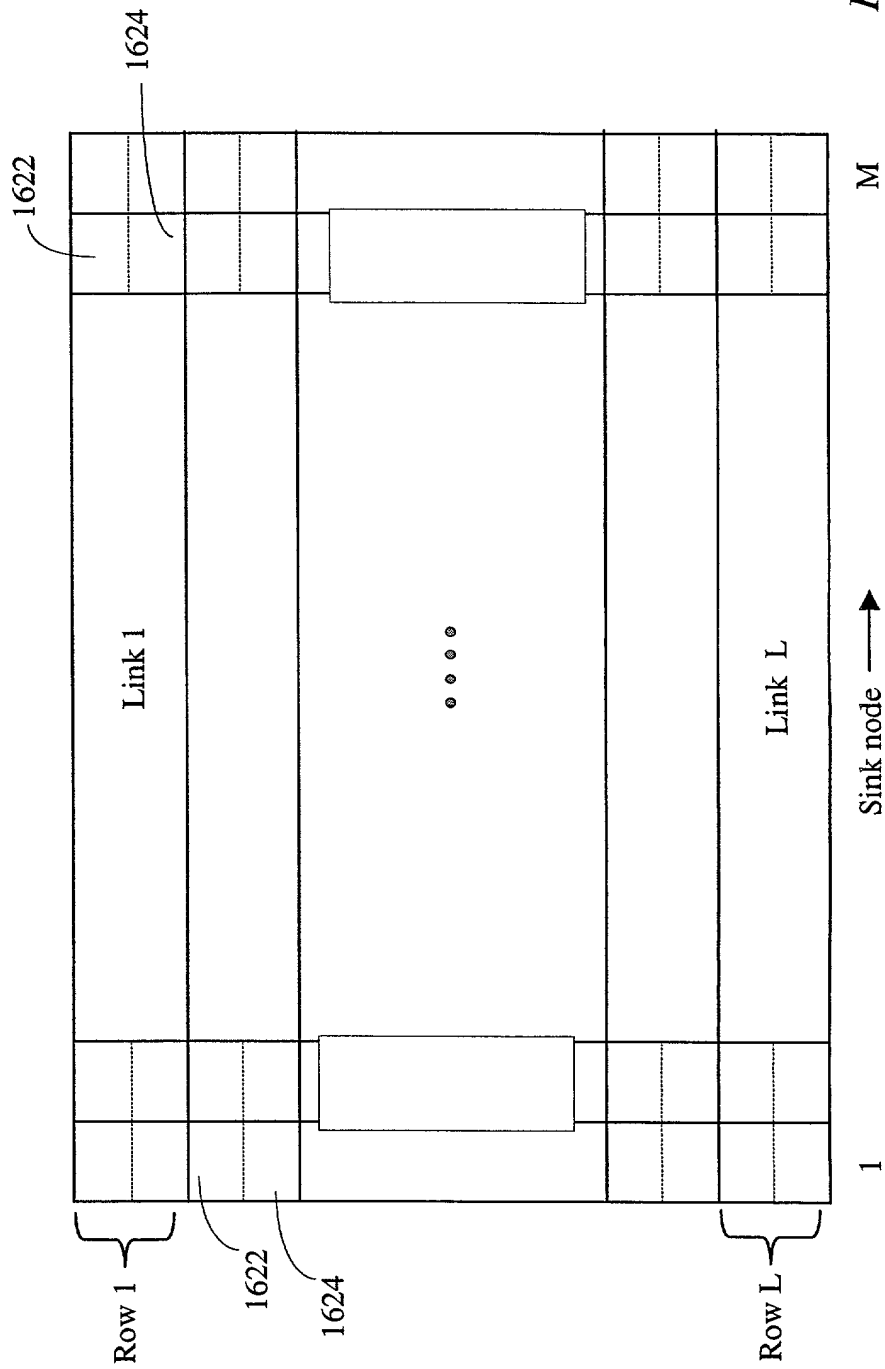


Fig. 16

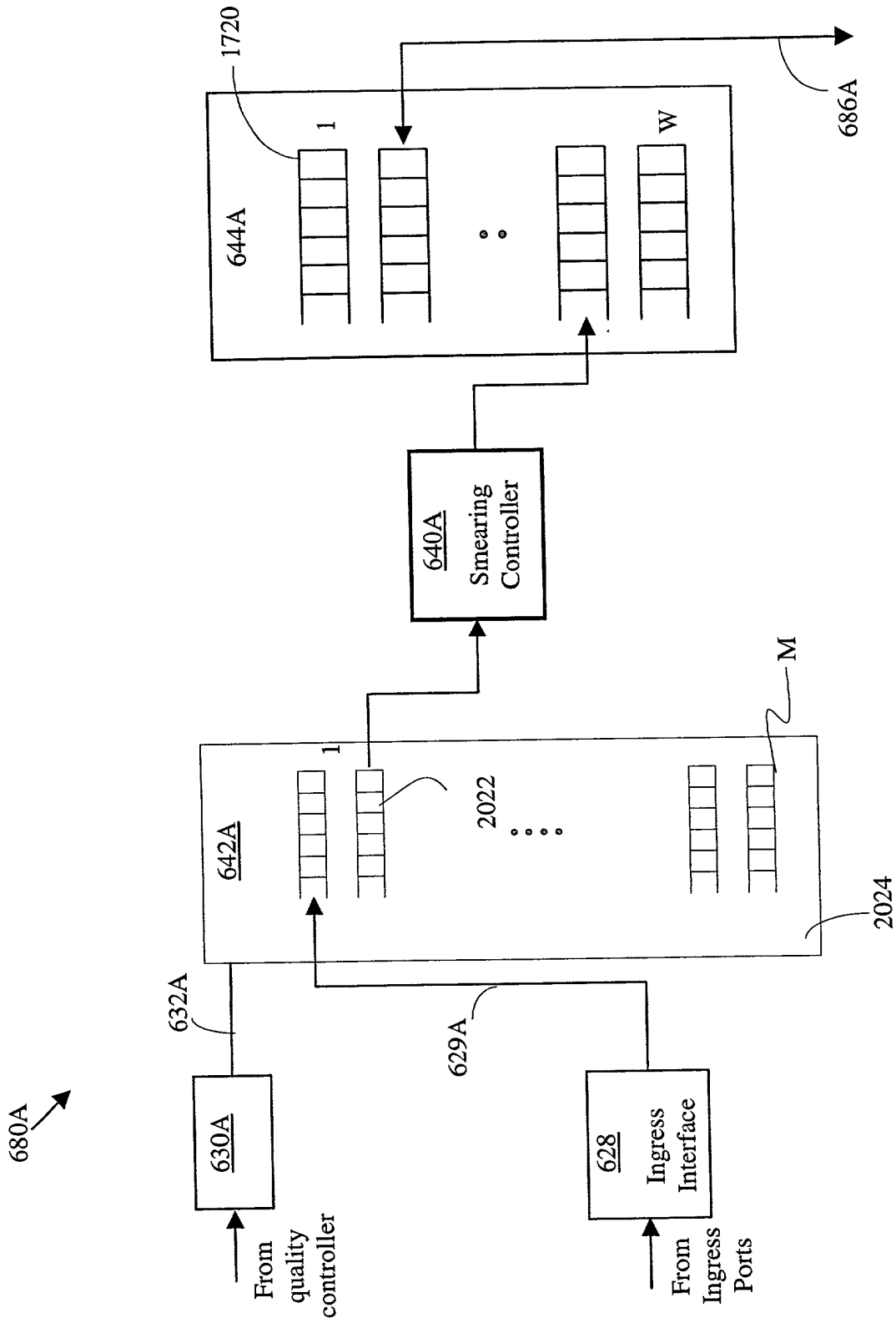


Fig. 17



FIG. 18 is a block diagram of a system 1800 for selecting a channel for a link. The system 1800 includes a processor 1810, a memory 1820, and a communication interface 1830. The processor 1810 is configured to receive a set of channels 1840 and a set of links 1850. The processor 1810 is also configured to select a channel 1860 from the set of channels 1840 based on a selection criterion 1870. The processor 1810 is further configured to assign the selected channel 1860 to a link 1880 from the set of links 1850. The processor 1810 is also configured to output a selection result 1890. The memory 1820 is configured to store the set of channels 1840, the set of links 1850, the selection criterion 1870, and the selection result 1890. The communication interface 1830 is configured to receive the set of channels 1840 and the set of links 1850, and to output the selection result 1890.

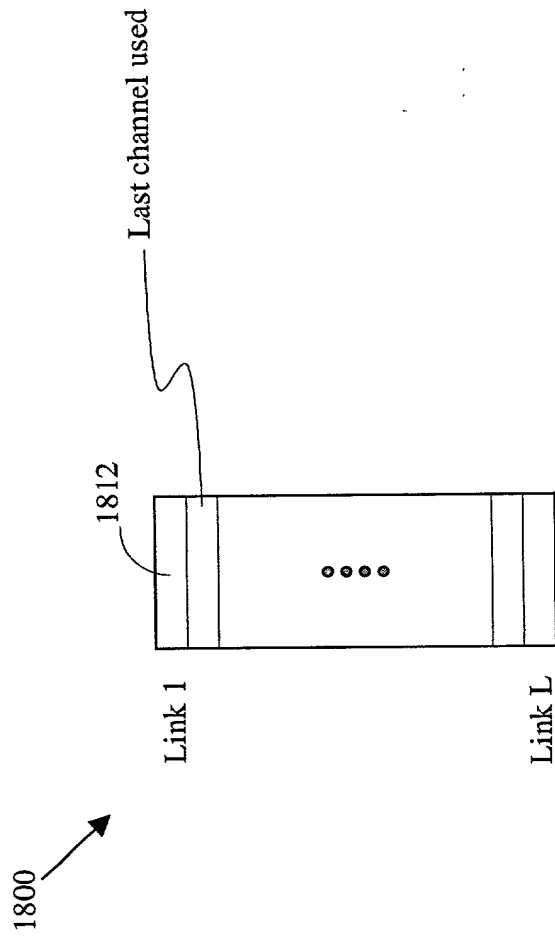


Fig. 18



FIG. 19 is a schematic diagram of a system 1900, which includes a plurality of links 1920, each having a plurality of segments 1922. The links 1920 are connected to a central hub 1924, which is configured to receive and transmit data to the links 1920. The links 1920 are arranged in a circular pattern around the central hub 1924, and each link 1920 is connected to the central hub 1924 via a cable 1926. The links 1920 are further connected to a plurality of devices 1928, which are arranged in a circular pattern around the links 1920. The devices 1928 are connected to the links 1920 via a cable 1930.

1900

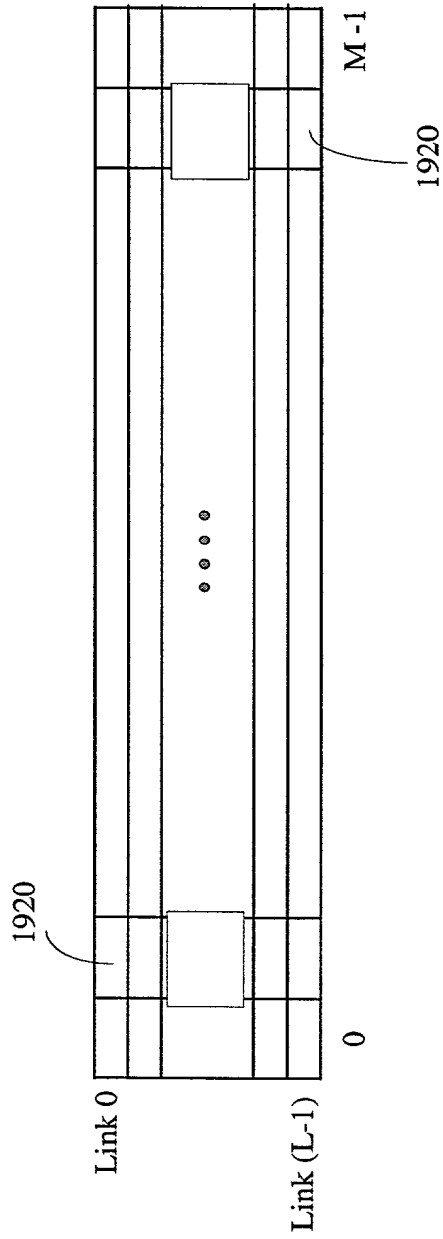


Fig. 19